ADCTRIG PAGE 1

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3 ; Author : ADI - Apps

4 ;

5 ; Date : Sept. '99

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7 ; File : adctrig.asm

8 ;

9 ; Description : Flash led an initial rate of 100ms

10 ; Pressing INTO triggers single conversion

11 ; The ADC result is written to external memory

12 ; The delay rate is increased

13 ; The program waits for the next INTO to repeat the

14 ; above sequence

15 ;

16 ;======================================================================

17 ;

18 $MOD824 ; Use ADuC824 predefined Symbols

19

0000 20 FLAG EQU 00H ; Define Bit

21

---- 22 CSEG ; Defines the following as a segment of code

23

0000 24 ORG 0000H ; Load Code at '0'

25

0000 020057 26 JMP MAIN ; Jump to MAIN

27

28 ;======================================================================

29

0003 30 ORG 0003h ; (INT0 ISR)

0003 F5F0 31 MOV B,A ; Copy A (sets delay)

0005 04 32 INC A ; Increment delay

33

0006 75D122 34 MOV ADCMODE,#22H ; INITIATE A MAIN ADC SINGLE CONVERSION

35

0009 30DFFD 36 JNB RDY0,$ ; Wait for conversion results

37

38 ; Write ADC Result H/M/L to ext. memory

000C 900000 39 MOV DPTR, #00H ; DPTR=00

000F E5D9 40 MOV A,ADC0L ; read ADC low byte

0011 F0 41 MOVX @DPTR,A ; write low byte to ext memory

0012 A3 42 INC DPTR ; DPTR=01

0013 E5DA 43 MOV A,ADC0M ; read ADC Middle byte

0015 F0 44 MOVX @DPTR,A ; write Middle byte to ext memory

0016 A3 45 INC DPTR ; DPTR=02

0017 E5DB 46 MOV A,ADC0H ; read ADC High byte

0019 F0 47 MOVX @DPTR,A ; write low High byte to ext memory

001A A3 48 INC DPTR

49

001B E5F0 50 MOV A,B ; Restore A (sets delay)

001D 04 51 INC A ; Increment delay

52

001E 32 53 RETI ; Return from Interrupt

54

55 ;======================================================================

56

57

004B 58 ORG 004Bh ; Subroutines

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59

60 ;------------------------------------------------------------------

61

004B 62 DELAY: ; Delays by 100ms \* A

63

004B F8 64 MOV R0,A ; Acc holds delay variable

004C 7919 65 DLY0: MOV R1,#019h ; Set up delay loop0

004E 7AFE 66 DLY1: MOV R2,#0FEh ; Set up delay loop1

0050 DAFE 67 DJNZ R2,$ ; Dec R2 & Jump here until R2 is 0

0052 D9FA 68 DJNZ R1,DLY1 ; Dec R1 & Jump DLY1 until R1 is 0

0054 D8F6 69 DJNZ R0,DLY0 ; Dec R0 & Jump DLY0 until R0 is 0

0056 22 70 RET ; Return from subroutine

71

72 ;======================================================================

73

0057 74 MAIN: ; (main program)

75

76 ; Configure ADC

0057 75D120 77 MOV ADCMODE,#20H ; ENABLE MAIN ADC; Mode- Power down

005A 75D247 78 MOV ADC0CON,#47H ; 24 BITS

79 ; USE EXTERNAL REFERENCE

80 ; AIN1-AIN2

81 ; BIPOLAR MODE

82 ; RANGE = +/-2.56V

83

005D D288 84 SETB IT0 ; INT0 edge triggered

005F D2AF 85 SETB EA ; enable inturrupts

0061 D2A8 86 SETB EX0 ; enable INT0

87

0063 C200 88 CLR FLAG ; Clear Bit defined as FLAG

89

0065 7401 90 MOV A,#01H ; Initialize A -> 1

0067 B2B4 91 BLINK: CPL P3.4 ; blink LED using compliment instruction

0069 114B 92 CALL DELAY ; Jump to subroutine DELAY

006B 3000F9 93 JNB FLAG,BLINK ; If FLAG is still cleared the jump to Blink

94

95 END

96

97

98

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

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ADC0CON. . . . . . . . . . . . . D ADDR 00D2H PREDEFINED

ADC0H. . . . . . . . . . . . . . D ADDR 00DBH PREDEFINED

ADC0L. . . . . . . . . . . . . . D ADDR 00D9H PREDEFINED

ADC0M. . . . . . . . . . . . . . D ADDR 00DAH PREDEFINED

ADCMODE. . . . . . . . . . . . . D ADDR 00D1H PREDEFINED

B. . . . . . . . . . . . . . . . D ADDR 00F0H PREDEFINED

BLINK. . . . . . . . . . . . . . C ADDR 0067H

DELAY. . . . . . . . . . . . . . C ADDR 004BH

DLY0 . . . . . . . . . . . . . . C ADDR 004CH

DLY1 . . . . . . . . . . . . . . C ADDR 004EH

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EX0. . . . . . . . . . . . . . . B ADDR 00A8H PREDEFINED

FLAG . . . . . . . . . . . . . . NUMB 0000H

IT0. . . . . . . . . . . . . . . B ADDR 0088H PREDEFINED

MAIN . . . . . . . . . . . . . . C ADDR 0057H

P3 . . . . . . . . . . . . . . . D ADDR 00B0H PREDEFINED

RDY0 . . . . . . . . . . . . . . B ADDR 00DFH PREDEFINED